WHAT IS CLAIMED IS:

1. An interface circuit provided for each of a first device set as a master side and a second device set as a slave side, for performing a serial data transmission between the first and second devices on the basis of a control signal which is output from the master side, comprising:

a first oscillation circuit which generates a first clock signal for data transmission upon receiving an operation-enable signal;

a transmission function portion which performs a serial data transmission with the other device upon receiving the first clock signal;

a second oscillation circuit which generates a second clock signal having a frequency lower than that of the first clock signal; and

a detection portion which detects the control signal on the basis of the second clock signal to output the operation-enable signal when a data transmission mode is designated by the control signal.

2. The interface circuit according to claim 1, wherein:

the first oscillation circuit includes a quartz oscillator, and the second oscillation circuit includes a CR oscillation circuit.

3. The interface circuit according to claim 1, wherein the detection portion comprises:

a shift register which shifts and holds the control signal in synchronization with the second clock signal, and;

a noise removal circuit which removes noise components contained in the control signal in accordance with logical addition and logical multiplication of the control signal held in the shift register.

4. An interface circuit provided for each of a first device set as a master side and a second device set as a slave side, for performing a serial data transmission between the first and second devices on the basis of a control signal which is output from the master side, comprising:

an oscillation circuit which generates a clock signal for data transmission upon receiving an operation-enable signal;

a transmission function portion which performs a serial data transmission with the other device upon receiving the clock signal;

a detection portion which monitors the control signal to output a detection signal when there is a change in the detection signal; and

a process control portion which performs control of the operation-enable signal on the basis of the detection signal.

5. The interface circuit according to claim 4, wherein the detection portion comprises:

a first flip-flop which is set at either one of the timings of a rise and a fall of the control signal;

a second flip-flop which holds an output signal of the first flip-flop;

a delay gate which delays an output signal of the second flip-flop by a predetermined time period; and

a comparator circuit which compares the output signal of the delay gate with the output signal of the first flip-flop to detect a change therein.

6. The interface circuit according to claim 4, wherein the detection portion comprises:

a register which holds an expected value supplied from the process control portion in accordance with the state of the control signal; and

a comparator circuit which compares the expected value held in the register with the control signal to output the detection signal on the basis of the comparison result;

wherein the process control portion is configured so as to perform control of the operation-enable signal in response to the detection signal, while re-writing the register value of the detection portion with the expected value for the next control signal in response to the detection signal.

7. The interface circuit according to claim 4, wherein the detection portion comprises:

a register which holds an expected value supplied from the process control portion in accordance with the state of the control signal in synchronization with the clock signal; and

a comparator circuit which compares the expected value held in the register with the control signal to output the detection signal on the basis of the comparison result;

wherein the process control portion is configured so as to perform control of the operation-enable signal in response to the detection signal, while supplying the expected value for

the next control signal to the register of the detection portion in response to the detection signal.

8. The interface circuit according to claim 6, wherein the detection portion comprises:

a noise removal circuit which removes noise components having short pulse widths contained in the control signal.